Atria Institute of Technology

Bengaluru – 560024

Approved by AICTE | Affiliated to VTU Belagavi | Accredited by NAAC

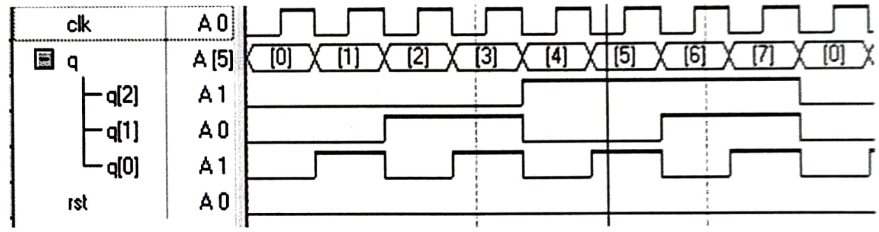
Department of Computer Science and Engineering

Date: 25/07/2018

DETAILS OF THE INNOVATIVE TEACHING METHODS USED BY THE FACULTY

Academic Year	2018-19, ODD SEM
Subject Name and Subject Code	Analog & Digital Electronics, 18CS33
Faculty Name	Hemalatha K N
Semester	III
Name of the Innovative Teaching Methods used	Hands-On Session On "Xilinx Software"
Short Description of the Innovative Teaching Activity.	VHDL stands for **Very HighSpeed Integrated Circuit Hardware Description Language.** It describes the behavior of an electronic circuit or system, from which the physical circuit or system can then be implemented. Intended students: 2nd year students **VHDL was originally intended to serve 2 main purposes-** 1. It was used as a **documentation** language for describing the structure of complex digital circuits. 2. VHDL provides features for modeling the **behavior** of a digital circuit. **General Features of VHDL:** 1. The language can be used as an exchange medium between chip vendors and CAD tool user and can be used as communication medium between CAD and CAE tools. 2. It supports hierarchy. 3. It is not a case sensitive language. 4. It is strongly type checked language. 5. It provides design portability and flexible design methodologies: top down,bottom up or mixed 6. It supports both synchronous and asynchronous timing models. 7. Nominal Propagation delays, min-max delays, setup and hold timing constraintand spike detection can be described in this language.

	Usage of the Tool: It is one of most popular software tools used to synthesize VHDL code. This toolincludes many steps. To make user feel comfortable with the tool the steps are given below:- **1.** Select NEW PROJECT in FILE MENU. a. Enter following details as per your convenience a. Project name: sample (should be same as the entity name in your VHDL code b. Project location : C:\example(As per convenience use default c. Top level module : HDL 2. In **NEW PROJECT** dropdown Dialog box, Choose your appropriate devicespecification. Example is given below: a. Device family : cyclone b. Device : EP1C6Q240 c. Package : PQFP d. Pincount :240 e. Speed grade 8 3. On File Drop down menu choose new Vhdl file. Type the Vhdl code Under the Processing Drop down menu 4. Choose Start compilation 5. If there are errors go back to the VHDL code and correct it. Once the compilationis successful 6. Under the processing drop down box select simulator tool select the simulator mode to functional and click on generate functional simulation netlist. we Get the success message. 7. Under simulator tool click on open. In the empty location right click. Click on insert on NODE or BUS. Then click on NODE finder. In the window opened select pins to unassigned. Click on List. IT will list all the Net list select all and click ok. 8. The input and output appear give appropriate input. 9. On the simulator tool click on start simulation. Simulation success message will beprompted.
Number of students got benefited.	40

Number of students involved in the activity.	60
Venue of the Activity	ADE lab
Date of the Event	23/07/2018 @12 PM
Whether the work can be Reproduced and Reviewed.	YES
Details are available in the college website.	YES
Photograph for the event	
Contents of the Event	Students simulated the circuits using Xilinx software and explored the practical working of theoretical circuits
Impact Analysis after using this Innovative Teaching Methods used.	Student's interest has been increased in designing the circuit in a different practical way
Feedback from the students	Amazing session -- No No. No Loved the session! Worthy Saturday morning!! Enjoyed and loved the session a lot It was really an interesting session hoping still many more sessions will be arranged.

	Enjoyed a lot in the session Still expecting someone knowledge It's very useful to me thank you ma'am None Loved the session. Would love to participate even more and learn more. It was the best session we want it more Now I'm enjoying my engineering life
Relevance to PO and PSO	PO3,PO5,PO9,PO10
Any comments or Suggestions from the Programme Co-ordinator	The content should be readily made in college website

Signature of the Faculty	**Signature of the HOD**
Hemalatha K N	Dr. Aishwarya. P Professor & Head CSE Atria Institute of Technology **Dr Aishwarya**